AMENDMENTS TO THE SPECIFICATION

Please substitute the following replacement paragraphs for the paragraphs that start at the specified page and line number within the present specification:

At page 2, line 4:

This application is a continuation-in-part of each of the following U.S. Patent Applications:

Application No. (U.S. Patent No.)		Filing Date
09/406,170		September 23, 1999
09/590,642	(6,324,087)	June 8, 2000
09/590,428	(6,763,425)	June 8, 2000
09/590,775	(6,687,785)	June 8, 2000
09/594,206	(6,801,981)	June 14, 2000
09/594,209	(6,813,680)	June 14, 2000
09/594,201	(6,799,243)	June 14, 2000
09/594,194	(6,751,701)	June 14, 2000
09/594,202	(6,795,892)	June 14, 2000
09/729,871		December 5, 2000
09/815,778		March 24, 2001
09/940,832	(6,542,391)	August 27, 2001

At page 75, line 16:

Numerous other implementations of the above described match flag logic, row match circuits, match one and group match circuits may be used in alternative embodiments. For example, U.S. Patent No. 6,542,391~~Application No. 09/940,832, filed August 27, 2001~~, which is hereby incorporated by reference in its entirety, describes at least one match flag logic embodiment that may be used in place of the above-described match flag logic.

At page 81, line 10:

Numerous other implementations of the above described priority encoder logic may be used in alternative embodiments. For example, U.S. Patent ~~Application~~ No. 6,542,391~~09/940,832~~, describes at least one priority encoder logic embodiment that may be used in place of the above-described priority encoder logic.

At page 86, line 9:

Each of the gating circuits 6203_1-6103_K is coupled to receive a respective block select signal 6016 from the corresponding comparator circuit 6207 and the block configuration signal from the corresponding block configuration register 6205. Each gating circuit 6203 includes logic to output a respective one of the multi-bit block configuration signals 6018_1-6018_K in accordance with the stored block configuration value if the corresponding block select signal 6016 is asserted. If the corresponding block select signal 6016 is not asserted, the block configuration signal 6018 is masked, for example, by forcing all component signals (not shown in Figure 62) of the block configuration signal 6018 to a logic low state. In alternative embodiments, the gating circuits 6203 are omitted so that the block configuration signals 6018_1-6018_K are output to respective block priority encoders 6005 and block flag circuits 6007 regardless of the state of the corresponding block select signals 6016_1-6016_K. In such alternative embodiments, it may be necessary to gate the signals generated by block flag circuits and/or block priority encoders according to the state of the corresponding block select signal. Such embodiments are described in U.S. Patent ~~Application~~ No. 6,542,391~~09/940,832~~.